

TMDS Regenerators with Multiplexers

The ISL54100, ISL54101, ISL54102 are high-performance TMDS timing regenerators and multiplexers. The receiver contains a programmable equalizer and a clock data recovery (CDR) function for each of the 3 TMDS pairs in an HDMI or DVI signal. The TMDS data outputs of the ISL54100 are regenerated and perfectly aligned to the regenerated TMDS clock signal, creating an extremely clean, low-jitter DVI/HDMI signal that can be easily decoded by any TMDS receiver.

The ISL54100's design and package footprint supports many compound configurations. Two ISL54100s can create a DualLink 4:1 mux, a 4:2 crosspoint, or an 8:1 mux. Additional ISL54100s can create larger combinations of these building blocks. The ISL54102 with its 2:1 multiplexing function serves applications with fewer inputs, while the ISL54101 can be used as a cable extender, to clean up a noisy/jittery TMDS source, or to provide a very stable TMDS signal to a finicky DVI receiver.

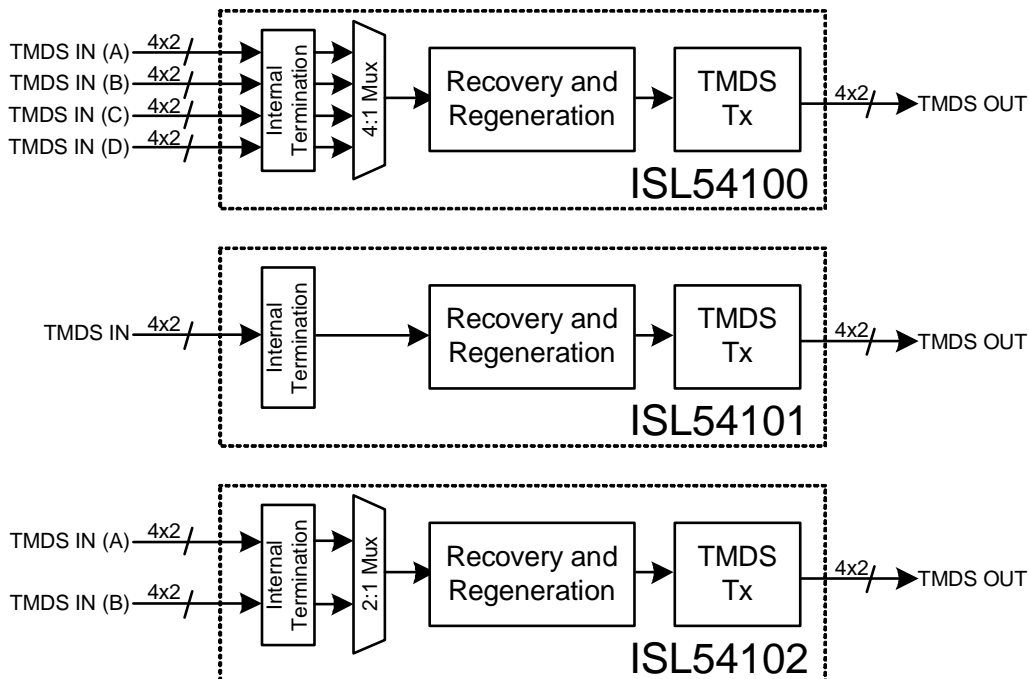
Features

- ISL54100: 4:1 TMDS regenerator and multiplexer
- ISL54101: 1:1 TMDS regenerator
- ISL54102: 2:1 TMDS regenerator and multiplexer
- Clock Data Recovery and Retiming function enables use as TMDS range extender
- Programmable pre-emphasis on output driver
- Channel activity detect based on input TMDS clock activity
- Symmetrical pinout enables high-performance DualLink, 4:2 crosspoint, and 8:1 multiplexing options
- Programmable internal 50Ω, 100Ω, or high-Z termination
- External pins for channel select, activity
- Stand-alone or software-controlled operation
- Hardware, software, or automatic channel selection
- Pb-free plus anneal available (RoHS compliant)

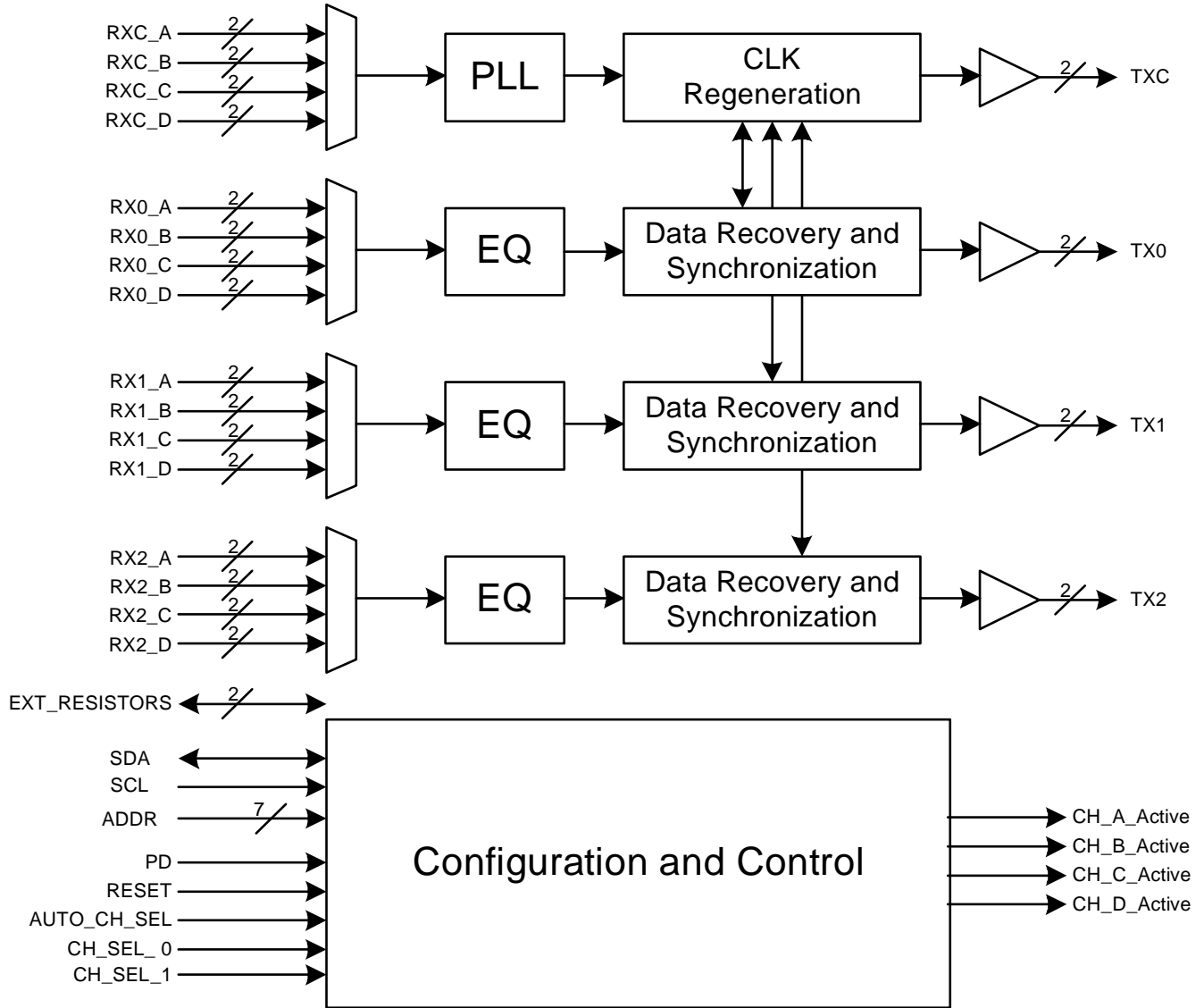
Applications

- KVM switches
- A/V receivers
- DVI/HDMI extenders
- Televisions/PC monitors/projectors

Block Diagrams



Block Diagram of ISL54100 (ISL54101, ISL54102 identical except for number of channels)



Ordering Information

PART NUMBER (Note)	NUMBER OF CHANNELS	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54100CQZ	4	0 to 70	128 Ld MQFP	MDP0055
ISL54101CQZ	1	0 to 70	128 Ld MQFP	MDP0055
ISL54102CQZ	2	0 to 70	128 Ld MQFP	MDP0055

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

ISL54100, ISL54101, ISL54102

Absolute Maximum Ratings

Voltage on V_D (referenced to GND)	4.0V
Voltage on any Input Pin (referenced to GND)	-0.3V to $V_D+0.3V$
Voltage on any "5V Tolerant" Input Pin (referenced to GND)	-0.3V to +6.0V
Current into any Output Pin	$\pm 20mA$
ESD Classification	
Human Body Model	2000V
Machine Model	200V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)
MQFP Package	30
Maximum Biased Junction Temperature	125°C
Storage Temperature	-65°C to +150°C

Recommended Operating Conditions

Temperature	0°C to +70°C
Supply Voltage	$V_D = 3.3V$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Specifications apply for $V_D = 3.3V$, pixel rate = 165MHz, $T_A = 25^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	COMMENT	MIN	TYP	MAX	UNIT
FULL CHANNEL CHARACTERISTICS						
	Rx Clock Frequency		25		165	MHz
	Rx Clock Duty Cycle		20		80	%
	Clock Jitter Tolerance		TBD			ps p-p
	Differential Input Sensitivity		TBD		TBD	mVp-p
	Rx Intra-Pair (+ to -) Differential Skew				TBD	UI
	Rx Inter-Pair (channel-to-channel) Skew					UI
	Tx Output Rise Time with 50Ω Load	20% to 80%	TBD		TBD	ps
	Tx Output Fall Time With 50Ω Load	20% to 80%	TBD		TBD	ps
	Tx Intra-Pair (+ to -) Differential Skew				TBD	UI
	Tx Inter-Pair (channel-to-channel) Skew					UI
TMDS INPUT CHARACTERISTICS						
	Termination Resistance Accuracy	Relative to external RES_TERM resistor value divided by 20		± 1	$\pm TBD$	%
TMDS OUTPUT CHARACTERISTICS						
SCHMITT DIGITAL INPUT CHARACTERISTICS						
V_{T+}	Low to High Threshold Voltage		1.45			V
V_{T-}	High to Low Threshold Voltage				0.95	V
I	Input Leakage Current			± 10		nA
	Internal Pull-Up Resistance	(SDA and SCL only)		70		kΩ
	Internal Pull-Down Resistance	(RESET only)		56		kΩ
	Input Capacitance			5		pF
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	Output HIGH Voltage, $I_O = 8mA$		2.4			V
V_{OL}	Output LOW Voltage, $I_O = -8mA$				0.4	V
POWER SUPPLY REQUIREMENTS						
V_D	Supply Voltage		3	3.3	3.6	V
I_D	Digital Supply Current			TBD	TBD	mA
P_D	Total Power Dissipation	With grayscale ramp input		TBD	TBD	W

Electrical Specifications Specifications apply for $V_D = 3.3V$, pixel rate = 165MHz, $T_A = 25^\circ C$, unless otherwise noted **(Continued)**

SYMBOL	PARAMETER	COMMENT	MIN	TYP	MAX	UNIT
AC TIMING CHARACTERISTICS (2-WIRE INTERFACE)						
f_{SCL}	SCL Clock Frequency		0		400	kHz
	Maximum Width of a Glitch on SCL that will be Suppressed	2 XTAL periods min	80			ns
t_{AA}	SCL LOW to SDA Data Out Valid	5 XTAL periods plus SDA's RC time constant			See comment	μs
t_{BUF}^+	Time the Bus Must be Free Before a New Transmission Can Start		1.3			μs
t_{LOW}	Clock LOW Time		1.3			μs
t_{HIGH}	Clock HIGH Time		0.6			μs
$t_{SU:STA}$	Start Condition Setup Time		0.6			μs
$t_{HD:STA}$	Start Condition Hold Time		0.6			μs
$t_{SU:DAT}$	Data In Setup Time		100			ns
$t_{HD:DAT}$	Data In Hold Time		0			ns
$t_{SU:STO}$	Stop Condition Setup Time		0.6			μs
t_{DH}	Data Output Hold Time	4 XTAL periods min	160			ns

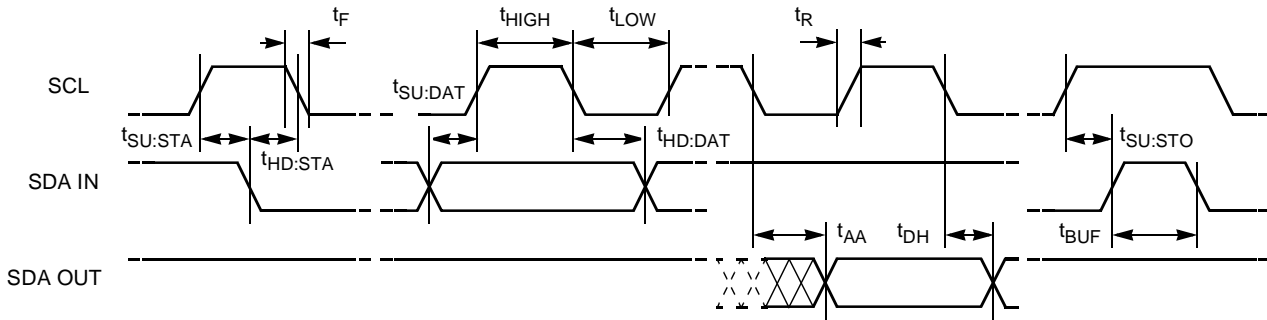
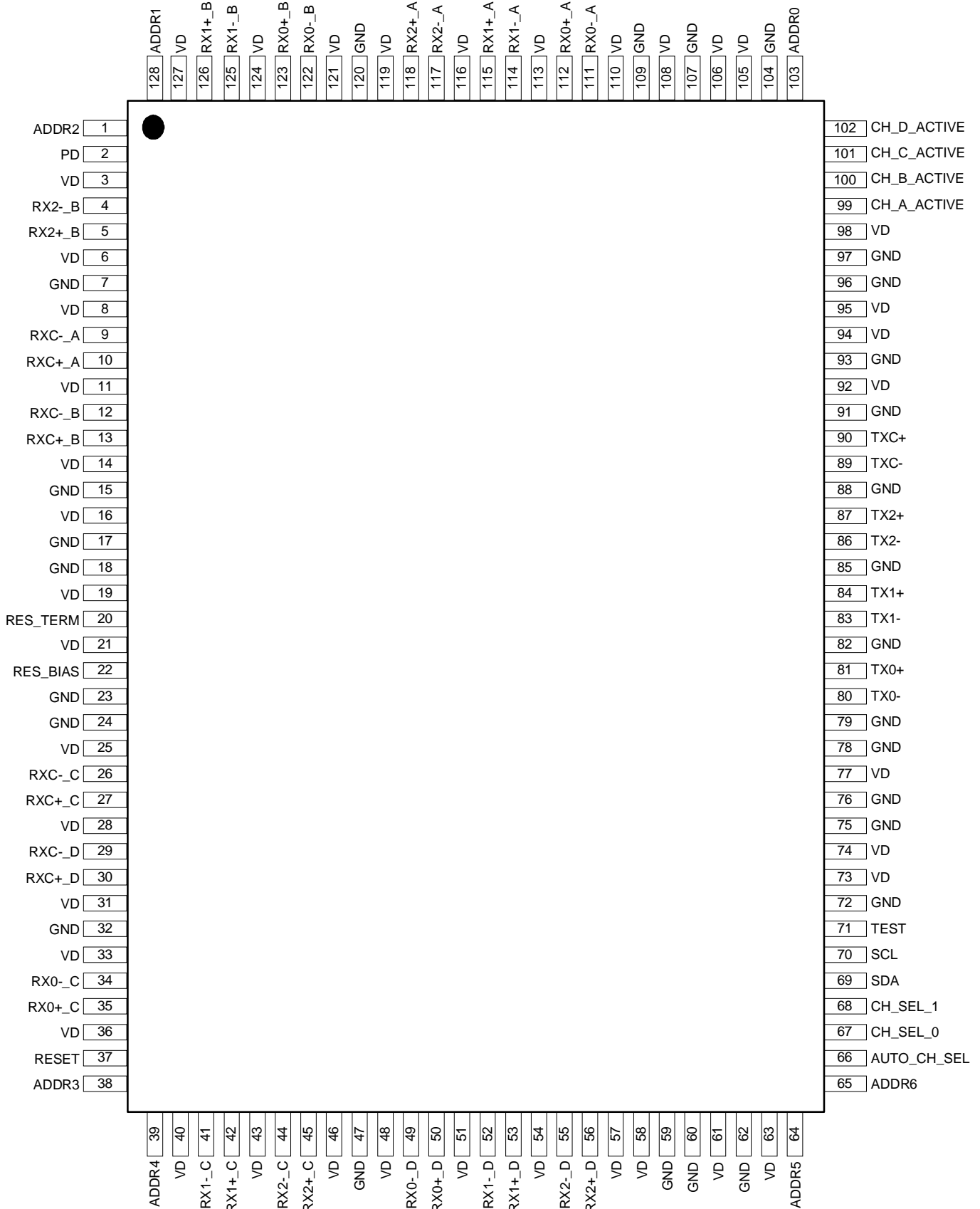
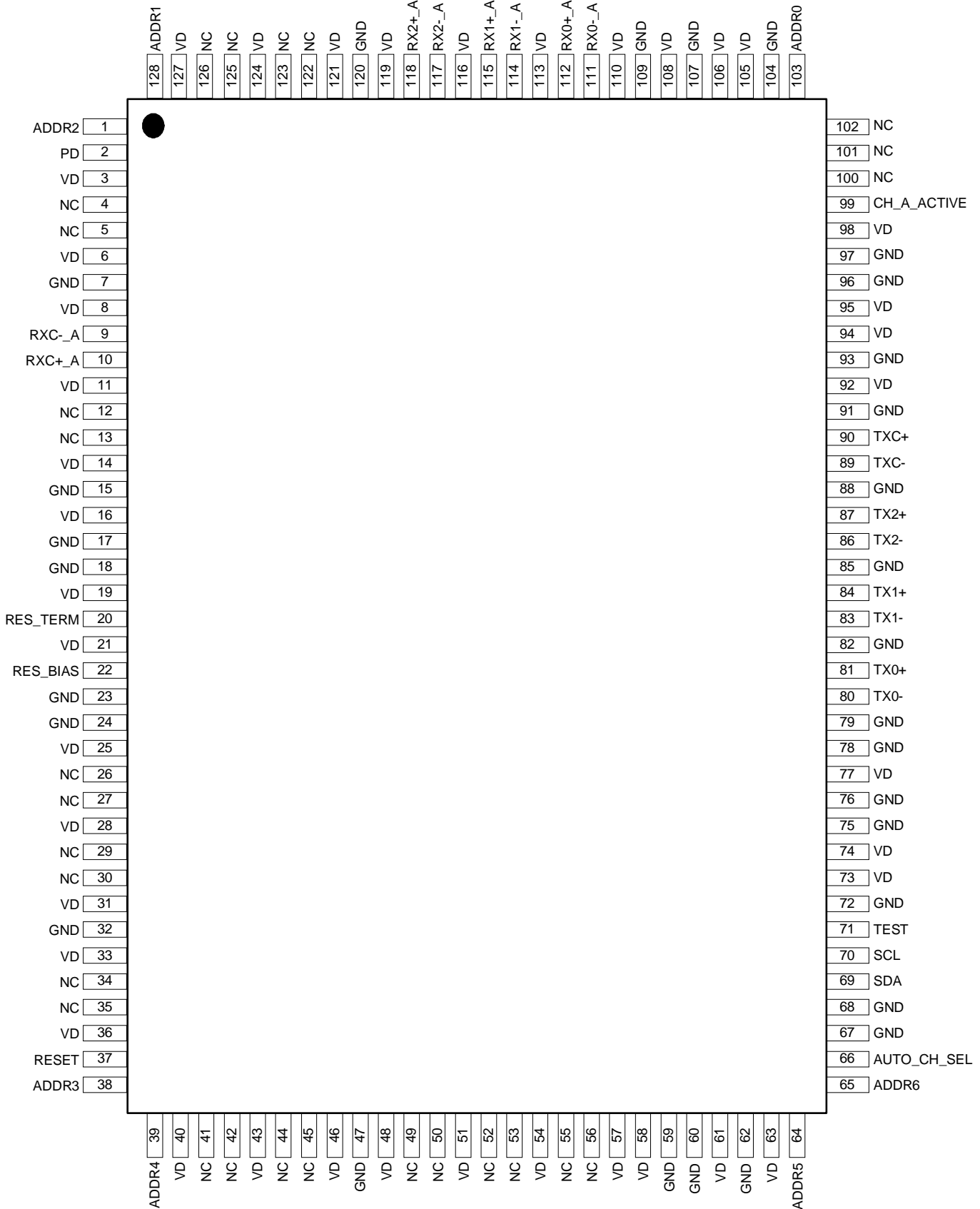


FIGURE 1. 2-WIRE INTERFACE TIMING

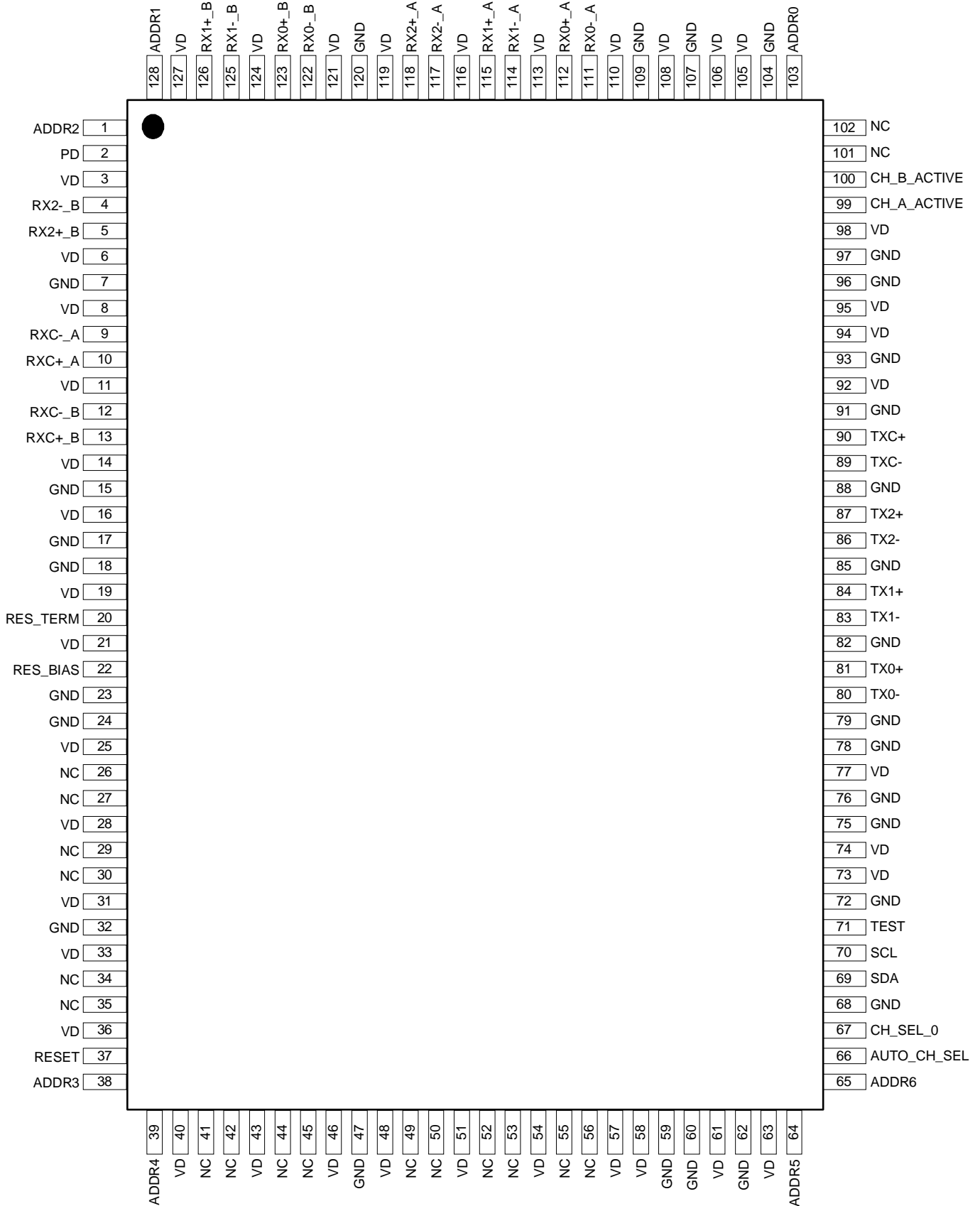
ISL54100 Pin Configuration



ISL54101 Pin Configuration



ISL54102 Pin Configuration



Pin Descriptions

SYMBOL	DESCRIPTION
RX0-_A, RX0+_A, RX1-_A, RX1+_A, RX2-_A, RX2+_A	TMDS Inputs. Incoming DVI data signals for channel A.
RX0-_B, RX0+_B, RX1-_B, RX1+_B, RX2-_B, RX2+_B	TMDS Inputs. Incoming DVI data signals for channel B (ISL54100 and ISL54102 only).
RX0-_C, RX0+_C, RX1-_C, RX1+_C, RX2-_C, RX2+_C	TMDS Inputs. Incoming DVI data signals for channel C (ISL54100 only).
RX0-_D, RX0+_D, RX1-_D, RX1+_D, RX2-_D, RX2+_D	TMDS Inputs. Incoming DVI data signals for channel D (ISL54100 only).
RXC-_A, RXC+_A, RXC-_B, RXC+_B, RXC-_C, RXC+_C, RXC-_D, RXC+_D	TMDS Inputs. Incoming DVI clock signals for channels A, B, C, and D (ISL54100), channels A and B (ISL54102), or channel A (ISL54101).
TX0-, TX0+, TX1-, TX1+, TX1-, TX1+	TMDS Outputs. DVI output data for selected channel.
TXC-, TXC+	TMDS Outputs. DVI output clock for selected channel.
SCL	Digital input, 5V tolerant, 500mV hysteresis. Serial data clock for 2-wire interface.
SDA	Bidirectional Digital I/O, open drain, 5V tolerant. Serial data I/O for 2-wire interface.
ADDR[6:0]	Digital inputs, 5V tolerant. 7-Bit address for serial interface.
CH_SEL_0, CH_SEL_1	Digital I/Os, 3.3V. Channel select inputs (for stand-alone operation), selected channel outputs (for software configured or auto channel select modes). CH_SEL_1 must be tied to GND for ISL54102. CH_SEL_0 and CH_SEL_1 must be tied to GND for ISL54101.
AUTO_CH_SEL	Digital Input. Pull high to have the mux automatically select the highest channel (A is highest, D is lowest) with an active TMDS clock. Low is manual channel select.
CHA_Active, CHB_Active, CHC_Active, CHD_Active	Digital Outputs, 3.3V. Output goes high when there is an active TMDS clock on that channel's input. Used for activity detect in a stand-alone configuration. CHC_Active and CHD_Active are NC (do Not Connect) for the ISL54102. CHB_Active, CHC_Active and CHD_Active are NC (do Not Connect) for the ISL54101.
RES_BIAS	Tie to GND through a 3.16k external resistor. Sets up internal bias currents.
RES_TERM	Tie to VD through a 1k external resistor. Nominal termination resistance = RES_TERM/20 = 50Ω.
PD	Pull high to put the ISL5410x in a minimum power consumption mode.
RESET	Pull high then low to reset the mux (should not be needed in normal operation).
V _D	Power supply. Connect to a 3.3V supply and bypass each pin to GND with 0.1μF.
GND	Ground return for V _D .

Register Listing

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x00	Device ID (read only)	3:0	Device Revision	1 = initial silicon, 2 = second revision, etc.
		7:4	Device ID	3 = ISL5410x
0x01	Channel Activity Detect (read only)	0	Channel A Active	0: TMDS clock not present on Channel A 1: TMDS clock detected on Channel A
		1	Channel B Active	0: TMDS clock not present on Channel B 1: TMDS clock detected on Channel B
		2	Channel C Active	0: TMDS clock not present on Channel C 1: TMDS clock detected on Channel C
		3	Channel D Active	0: TMDS clock not present on Channel D 1: TMDS clock detected on Channel D
0x02	Channel Selection (0x0C)	1:0	Channel Select	Selects the input channel for the mux. These 2 bits are Read Only if Auto Channel Select is enabled. 0: Channel A selected 1: Channel B selected 2: Channel C selected 3: Channel D selected
		2	Auto Channel Select	0: Manual Select Channel 1: Auto-Select based on most recent inactive-to-active channel activity. If the active channel becomes inactive, channel selection stays the same (until/unless a different channel changes from inactive-to-active). (default)
		3	Hardware Channel Select	0: Software channel selection (using bits 0-2 of this register) 1: Hardware channel selection (using "Auto Channel Select" and "CH Sel 0/1" external pins) (default)
		4	Reset	Full chip reset. Write a 1 to reset. Will set itself to 0 when reset is complete.
		5	Power Down	0: Normal Operation 1: Puts the chip in a minimal power consumption mode, turning off all TMDS outputs and open-circuiting all TMDS inputs. This bit is OR'ed with the Power Down input pin. If either is set, the chip will enter power down. Serial I/O stays operational in PD mode.

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x03	Input Control (0x12)	0	Tristate Unselected Clock Inputs	0: Normal Operation 1: Termination of unselected TMDS clock inputs is tristated to save power. Setting this bit will disable the activity detect function. This bit should not be set in crosspoint configuration because it will make the clock termination resistance variable depending on which 2 inputs are selected. In general, this bit should always be set to 0.
		1	Tristate Unselected Data Inputs	0: Normal Operation 1: Unselected Data inputs are tristated to save power. This bit should not be set in crosspoint configuration because it will make the data input termination resistance variable depending on which 2 inputs are selected. (default)
		2	Tristate Selected Clock Inputs	0: Selected Clock inputs are terminated into 50Ω/100Ω. 1: Selected Clock inputs are tristated (to allow chip to operate in parallel with another TMDS receiver with fixed 50Ω termination)
		3	Tristate Selected Data Inputs	0: Selected Data inputs are terminated into 50Ω/100Ω. 1: Selected Data inputs are tristated (to allow chip to operate in parallel with another TMDS receiver with fixed 50Ω termination)
		4	Connection Check	0: Connection Check disabled. Activity detect is based only on presence of AC activity on TMDS clock inputs. 1: Connection Check enabled. If there is no TMDS source connected to a clock input, the activity detect for that input is always negative. This is to prevent false triggering of activity detect function due to noise on unconnected inputs. (default)
		5	Rx Hysteresis	0: TMDS input hysteresis disabled 1: TMDS input hysteresis enabled. Will reduce false activity detects on unconnected channels, but may reduce ability to recover the poorest quality input signals.
		6	Rx Hysteresis Magnitude	Controls the amount of hysteresis in the activity detect function. 0: 10mV 1: 20mV
		7	Recalibrate	0: Normal Operation 1: Recalibrates termination resistance. To recalibrate, take this bit high, wait at least 1ms, then take this bit low. Calibration is automatically done after power-on, so this function is not needed in normal operation.

Register Listing (Continued)

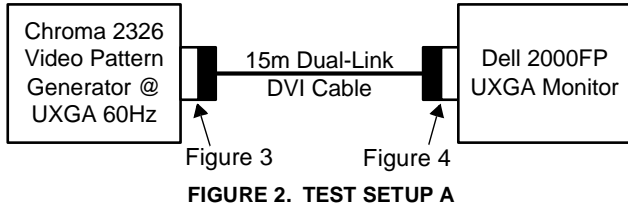
ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x04	Termination Control (0x00)	0	Data Termination A	0: Channel A TMDS Data inputs terminated into 50Ω (normal operation) 1: Channel A TMDS Data inputs terminated into 100Ω (for paralleled inputs)
		1	Data Termination B	0: Channel B TMDS Data inputs terminated into 50Ω (normal operation) 1: Channel B TMDS Data inputs terminated into 100Ω (for paralleled inputs)
		2	Data Termination C	0: Channel C TMDS Data inputs terminated into 50Ω (normal operation) 1: Channel C TMDS Data inputs terminated into 100Ω (for paralleled inputs)
		3	Data Termination D	0: Channel D TMDS Data inputs terminated into 50Ω (normal operation) 1: Channel D TMDS Data inputs terminated into 100Ω (for paralleled inputs)
		4	Clk Termination A	0: Channel A TMDS Clock inputs terminated into 50Ω (normal operation) 1: Channel A TMDS Clock inputs terminated into 100Ω (for paralleled inputs)
		5	Clk Termination B	0: Channel B TMDS Clock inputs terminated into 50Ω (normal operation) 1: Channel B TMDS Clock inputs terminated into 100Ω (for paralleled inputs)
		6	Clk Termination C	0: Channel C TMDS Clock inputs terminated into 50Ω (normal operation) 1: Channel C TMDS Clock inputs terminated into 100Ω (for paralleled inputs)
		7	Clk Termination D	0: Channel D TMDS Data inputs terminated into 50Ω (normal operation) 1: Channel D TMDS Data inputs terminated into 100Ω (for paralleled inputs)
0x05	Output Options (0x00)	0	Tristate Clock Outputs	0: Normal Operation 1: Clock outputs tristated (allows another chip to drive the output clock pins)
		1	Tristate Data Outputs	0: Normal Operation 1: Data outputs tristated (allows another chip to drive the output data pins)
		2	Invert Output Polarity	0: Normal Operation 1: The polarities of the TMDS outputs are inverted (+ becomes -, - becomes +).
		4	Reverse Output Order	0: Normal Operation 1: CH0 data is output on CH2, and CH2 data is output on CH0. No change to CH1.
0x06	Output Drive (0x00)	3:0	Transmit Current	Transmit Drive Current, adjustable in 0.125mA steps. 0x0: 10mA 0x8: 11mA 0xF: 11.875mA
		7:4	Transmit PreEmphasis	Drive boost (in 0.125mA steps) added during first half of each bit period. 0x0: 0mA 0x8: 1mA 0xF: 1.875mA

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x07	Equalization 1 (0xCC)	3:0	Channel A Equalizer Gain	0x0: Zero boost 0xF: Max boost
		7:4	Channel B Equalizer Gain	0x0: Zero boost 0xF: Max boost
0x08	Equalization 2 (0xCC)	3:0	Channel C Equalizer Gain	0x0: Zero boost 0xF: Max boost
		7:4	Channel D Equalizer Gain	0x0: Zero boost 0xF: Max boost
0x09	Test Pattern Generator (0x00)	1:0	Generator Mode	When a 25MHz to 165MHz clock is applied to the selected channel's clock input, this function will output a PRBS7 pattern on the TX pins. 0: Disabled 1: PRBS7 random generator 2: Low Frequency Pattern (0000011111...) 3: High Frequency Pattern (1010101010...)
		2	Enable PRBS7 Error Counter	Enables PRBS7 error counter in registers 0x0A-0x0C. 0: Disable PRBS7 Error Counter 1: Enable PRBS7 Error Counter
0x0A	PRBS7 Error Counter Link 0 (RO)	7:0	PRBS7 Error Counter Link 0	PRBS7 Error Counter of Link 0. Saturates at 0xFF. Reading this register clears this register at end of read
0x0B	PRBS7 Error Counter Link 1 (RO)	7:0	PRBS7 Error Counter Link 1	PRBS7 Error Counter of Link 1. Saturates at 0xFF. Reading this register clears this register at end of read
0x0C	PRBS7 Error Counter Link 2 (RO)	7:0	PRBS7 Error Counter Link 2	PRBS7 Error Counter of Link 2. Saturates at 0xFF. Reading this register clears this register at end of read

Typical Performance

Setup A (Figure 2) was used to capture the TMDS eye diagrams shown in Figure 3 and Figure 4:



The 162.5Mpixel/s (UXGA 60Hz) DVI output of the Chroma 2326 was terminated into a TPA2 Plug adapter and measured with a LeCroy differential probe and 6MHz SDA using the LeCroy's software clock recovery. As Figure 3 shows, the amplitude of the TMDS signal is slightly low, but the eye is otherwise acceptable.

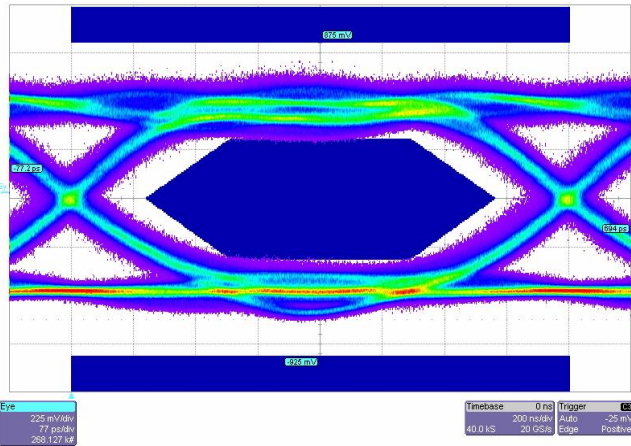


FIGURE 3. EYE DIAGRAM AT OUTPUT OF CHROMA GENERATOR

Next, a 15m DualLink DVI cable was attached and terminated into a female TPA2 adapter, and the eye captured in Figure 4.

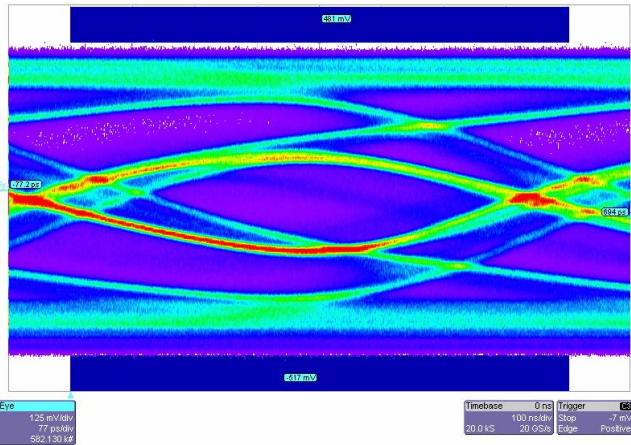
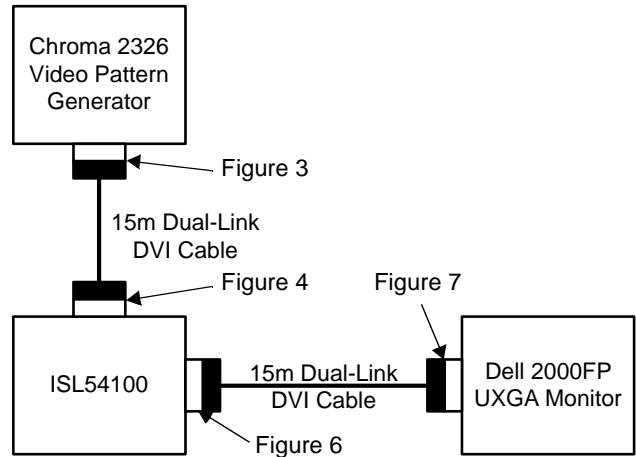


FIGURE 4. CHROMA EYE DIAGRAM AFTER 15m CABLE

The eye is not meeting the minimum requirements of either the HDMI or DVI standards, and the Dell Monitor is unable to recover the data and display an image.

Setup B inserts an ISL54100 and an additional 15m cable between the pattern generator and the monitor:



Given the input signal shown in Figure 4, the ISL54100's TMDS output signal (Figure 6) is extremely clean. The output is an improvement over the original signal coming from the pattern generator in both amplitude and jitter.

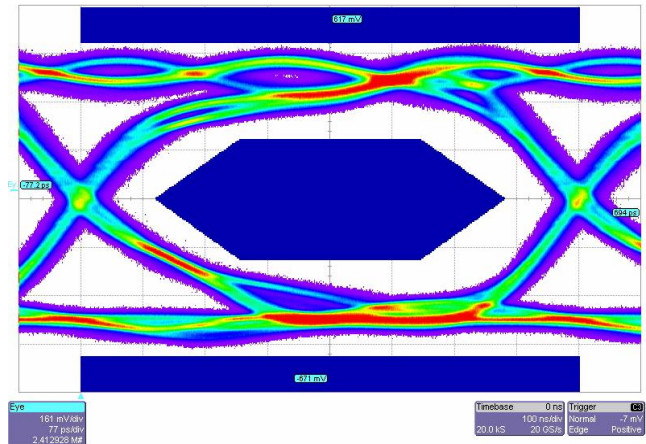


FIGURE 6. EYE DIAGRAM AT OUTPUT OF ISL54100

The cleaner signal generated at the output of the ISL54100 results in an improved eye at the end of another 15m cable (Figure 7). The eye is open enough that the Dell 2000FP can now display a UXGA image with no visible sparkle or other artifacts.

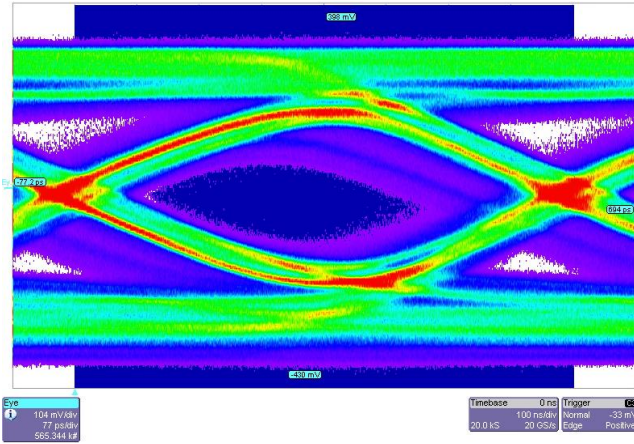


FIGURE 7. ISL54100 EYE DIAGRAM AFTER 15m CABLE

PCB Layout Recommendations

Because of the high speed of the TMDS signals, careful PCB layout is critical to maximize performance. The following guidelines should be adhered to as closely as possible:

- All TMDS pair traces should have a characteristic impedance of 50 ohms with respect to the power/ ground planes, and 100 ohms with respect to each other. Failure to meet this requirement will increase reflections, shavavailable eye.
- Avoid vias for all 3 high speed TMDS pairs. Keep all the traces on the top (or the bottom) of the PCB. The TMDS clock can have vias if necessary.
- Maintain a constant, solid ground (or power) plane under the 3 high speed TMDS signals. Do not route the signals over gaps in the ground plane or over other traces.
- For each DVI channel, the length of the 3 TMDS pairs (0, 1, and 2) should be the same. This reduces any interchannel skew introduced by the board. The clock pair is not as critical, since its frequency is 1/10th the pixel rate.

ISL5410x Serial Communication

Overview

The ISL5410x uses a 2-wire serial bus for communication with its host. SCL is the Serial Clock line, driven by the host, and SDA is the Serial Data line, which can be driven by all devices on the bus. SDA is open drain to allow multiple devices to share the same bus simultaneously.

Communication is accomplished in three steps:

- 1) The Host selects the ISL5410x it wishes to communicate with.
- 2) The Host writes the initial ISL5410x Configuration Register address it wishes to write to or read from.

- 3) The Host writes to or reads from the ISL5410x's Configuration Register. The ISL5410x's internal address pointer auto increments, so to read registers 0x00 through 0x1B, for example, one would write 0x00 in step 2, then repeat step three 28 times, with each read returning the next register value.

The ISL5410x has a 7-bit address on the serial bus. The upper 6-bits are permanently set to 100110, with the lower bit determined by the state of pin 48. This allows two ISL5410xs to be independently controlled while sharing the same bus.

The bus is nominally inactive, with SDA and SCL high. Communication begins when the host issues a START command by taking SDA low while SCL is high (Figure 8). The ISL5410x continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. The host then transmits the 7-bit serial address plus a R/\overline{W} bit, indicating if the next transaction will be a Read ($R/\overline{W} = 1$) or a Write ($R/\overline{W} = 0$). If the address transmitted matches that of any device on the bus, that device must respond with an ACKNOWLEDGE (Figure 9).

Once the serial address has been transmitted and acknowledged, one or more bytes of information can be written to or read from the slave. Communication with the selected device in the selected direction (read or write) is ended by a STOP command, where SDA rises while SCL is high (Figure 8), or a second START command, which is commonly used to reverse data direction without relinquishing the bus.

Data on the serial bus must be valid for the entire time SCL is high (Figure 10). To achieve this, data being written to the ISL5410x is latched on a delayed version of the rising edge of SCL. SCL is delayed and deglitched inside the ISL5410x for three crystal clock periods (120ns for a 25MHz crystal) to eliminate spurious clock pulses that could disrupt serial communication.

When the contents of the ISL5410x are being read, the SDA line is updated after the falling edge of SCL, delayed and deglitched in the same manner.

Configuration Register Write

Figure 11 shows two views of the steps necessary to write one or more words to the Configuration Register.

Configuration Register Read

Figure 12 shows two views of the steps necessary to read one or more words from the Configuration Register.

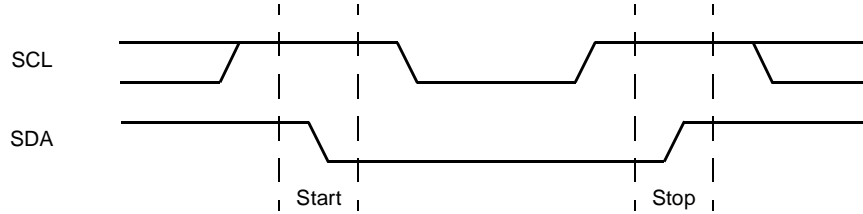


FIGURE 8. VALID START AND STOP CONDITIONS

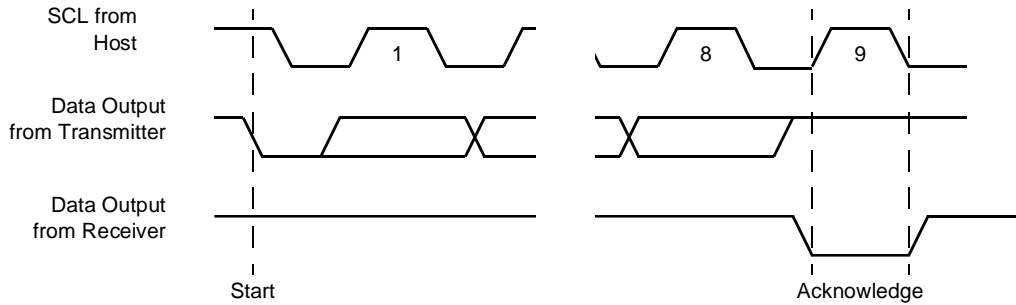


FIGURE 9. ACKNOWLEDGE RESPONSE FROM RECEIVER

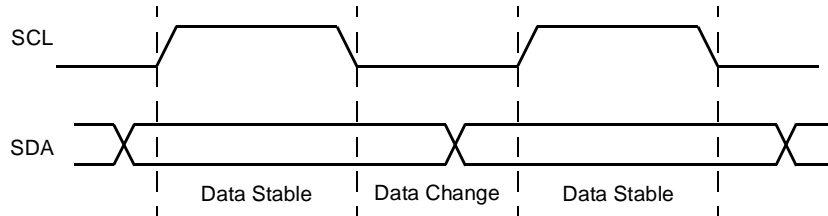


FIGURE 10. VALID DATA CHANGES ON THE SDA BUS

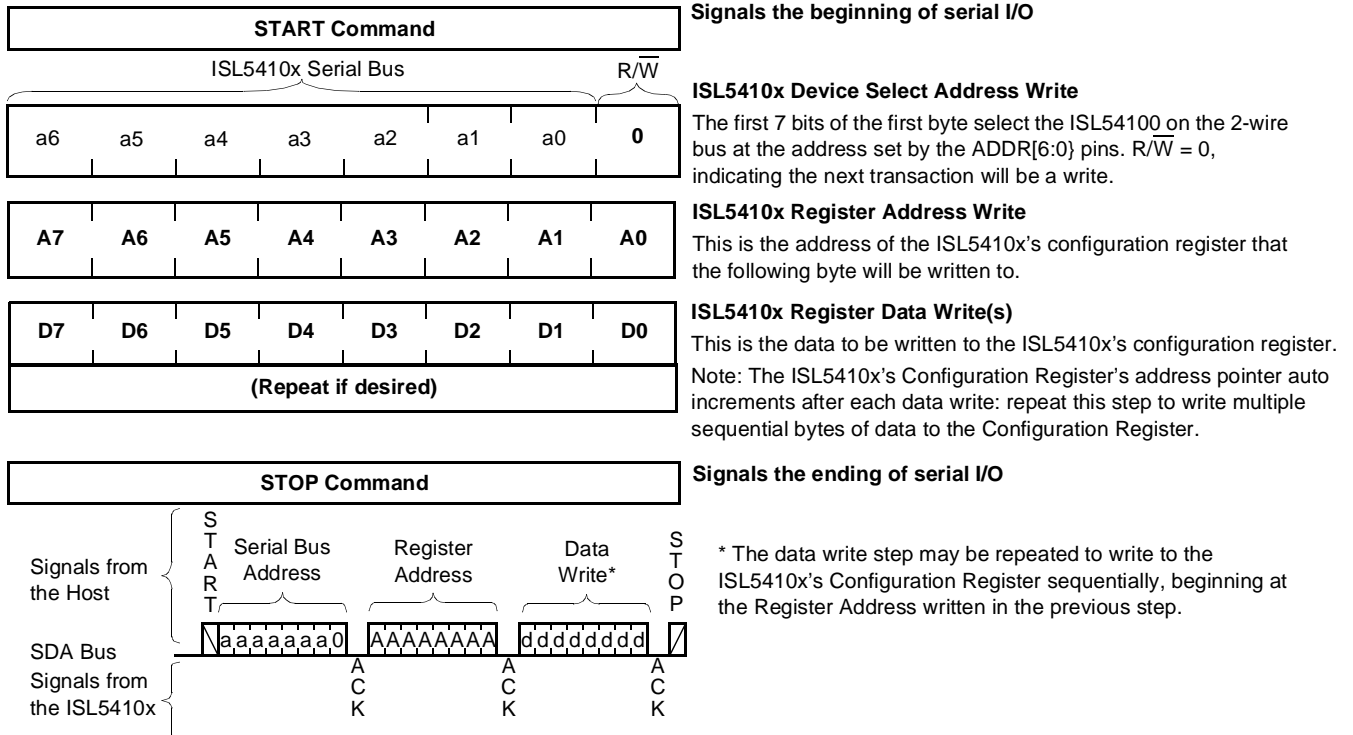


FIGURE 11. CONFIGURATION REGISTER WRITE

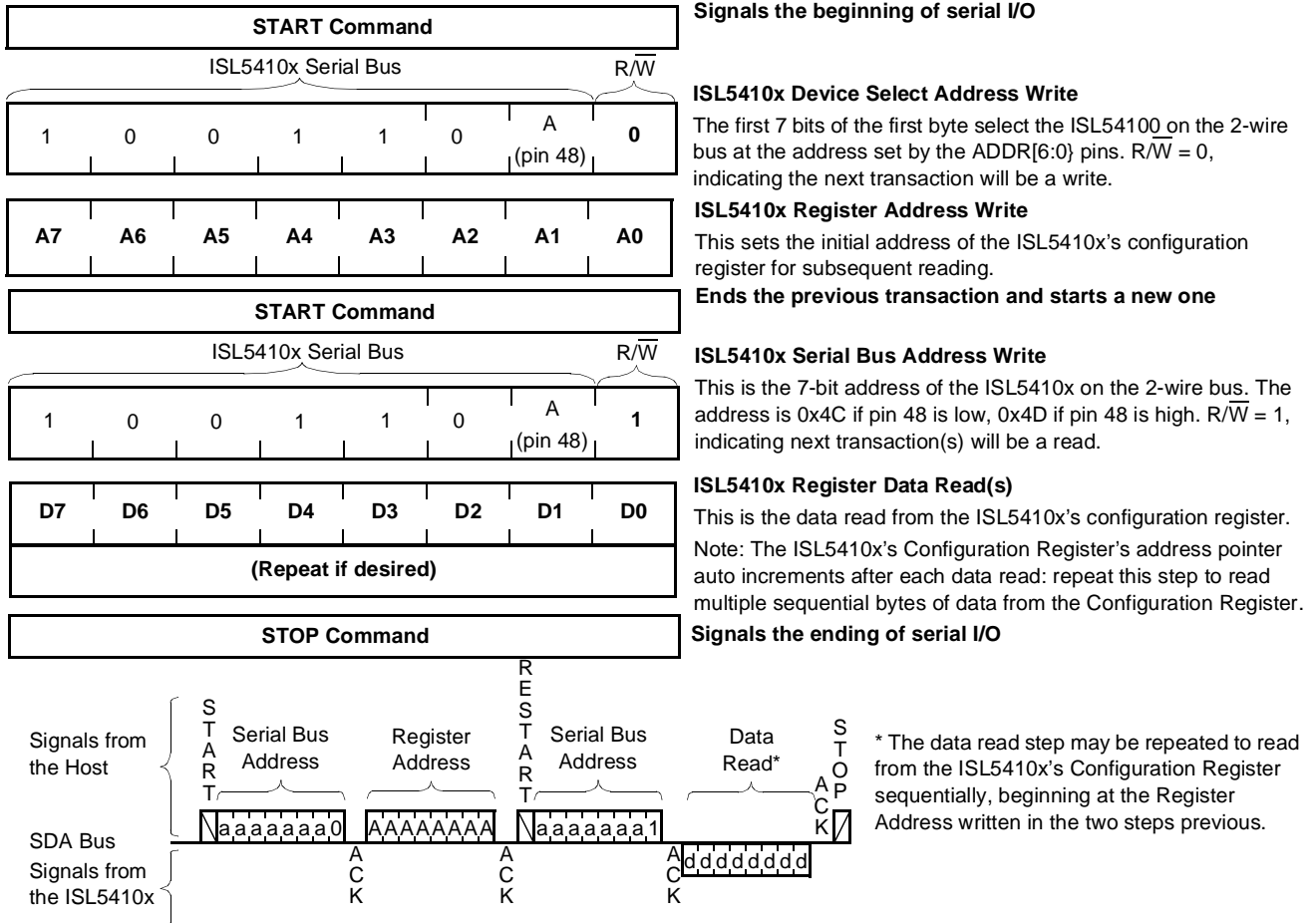


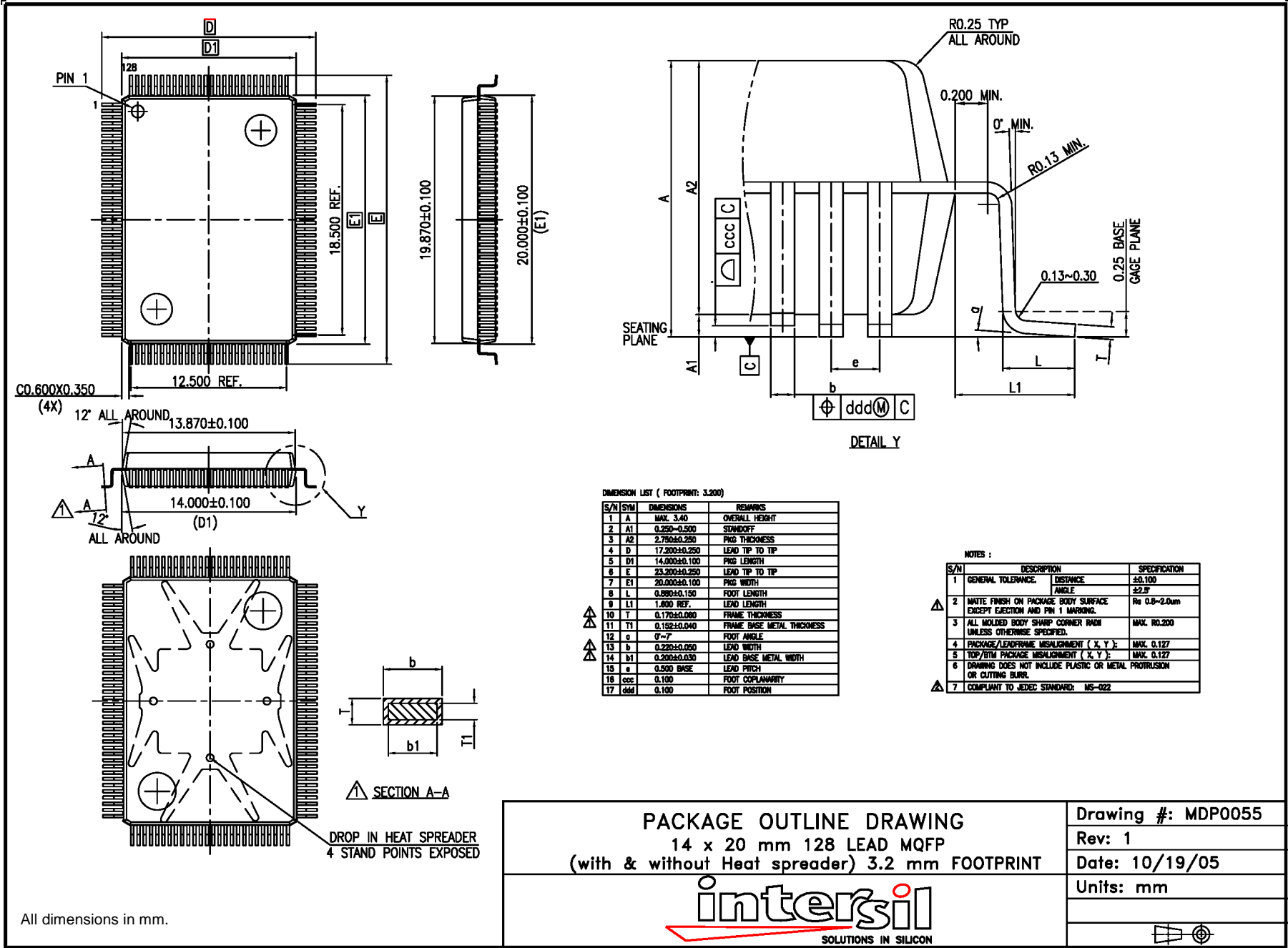
FIGURE 12. CONFIGURATION REGISTER READ

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

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128-Lead Metric Quad Flat Pack (MQFP) Package



DIMENSION LIST (FOOTPRINT: 3.200)

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 3.40	OVERALL HEIGHT
2	A1	0.250-0.500	STANDOFF
3	A2	2.750±0.250	PKG THICKNESS
4	D	17.200±0.250	LEAD TIP TO TIP
5	D1	14.000±0.100	PKG LENGTH
6	E	23.200±0.250	LEAD TIP TO TIP
7	E1	20.000±0.100	PKG WIDTH
8	L	0.800±0.150	FOOT LENGTH
9	L1	1.800 REF.	LEAD LENGTH
10	T	0.170±0.080	FRAME THICKNESS
11	T1	0.152±0.040	FRAME BASE METAL THICKNESS
12	θ	0~7	FOOT ANGLE
13	b	0.220±0.050	LEAD WIDTH
14	b1	0.200±0.030	LEAD BASE METAL WIDTH
15	φ	0.500 BASE	LEAD PITCH
16	ccc	0.100	FOOT COPLANARITY
17	ddd	0.100	FOOT POSITION

NOTES :

S/N	DESCRIPTION	SPECIFICATION
1	GENERAL TOLERANCE	DISTANCE ±0.100 ANGLE ±2.5°
2	WHITE FINISH ON PACKAGE BODY SURFACE EXCEPT EJECTION AND PIN 1 MARKING.	Ro 0.8-2.0um
3	ALL MOLDED BODY SHARP CORNER RADI UNLESS OTHERWISE SPECIFIED.	MAX. R0.200
4	PACKAGE/LEADFRAME MISALIGNMENT (X, Y):	MAX. 0.127
5	TOP/BTM PACKAGE MISALIGNMENT (X, Y):	MAX. 0.127
6	DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OR CUTTING BURR.	
7	COMPLIANT TO JEDEC STANDARD: MS-022	

PACKAGE OUTLINE DRAWING
14 x 20 mm 128 LEAD MQFP
(with & without Heat spreader) 3.2 mm FOOTPRINT

Drawing #: MDP0055
Rev: 1
Date: 10/19/05
Units: mm



All dimensions in mm.